

FIG. 1

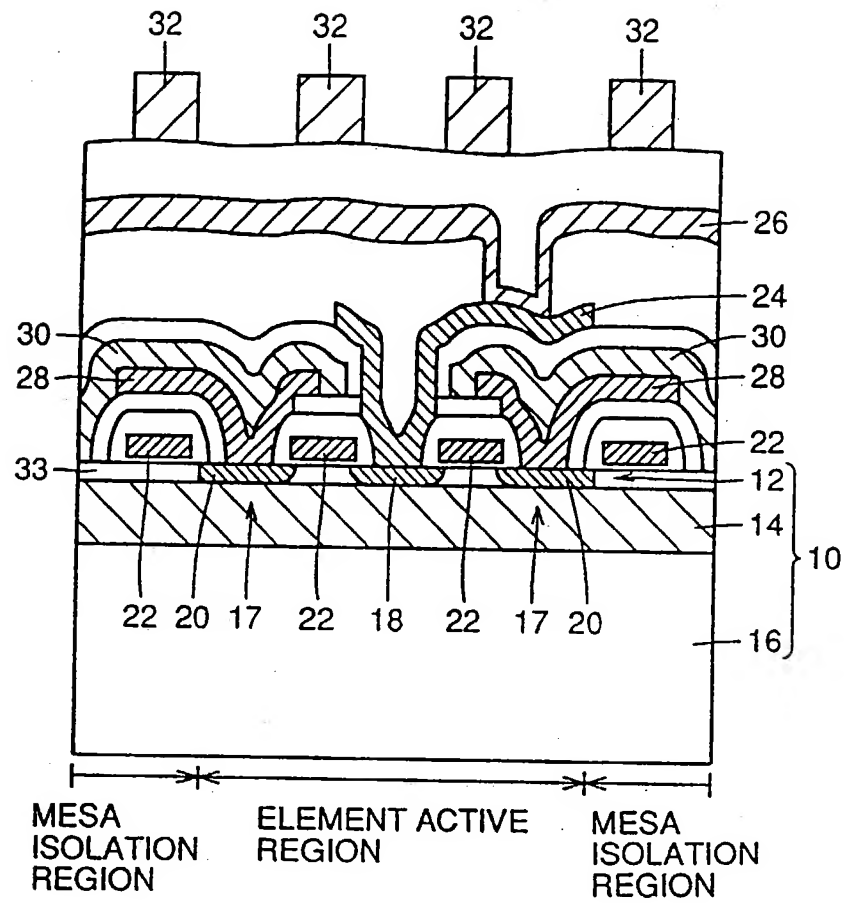


FIG.2

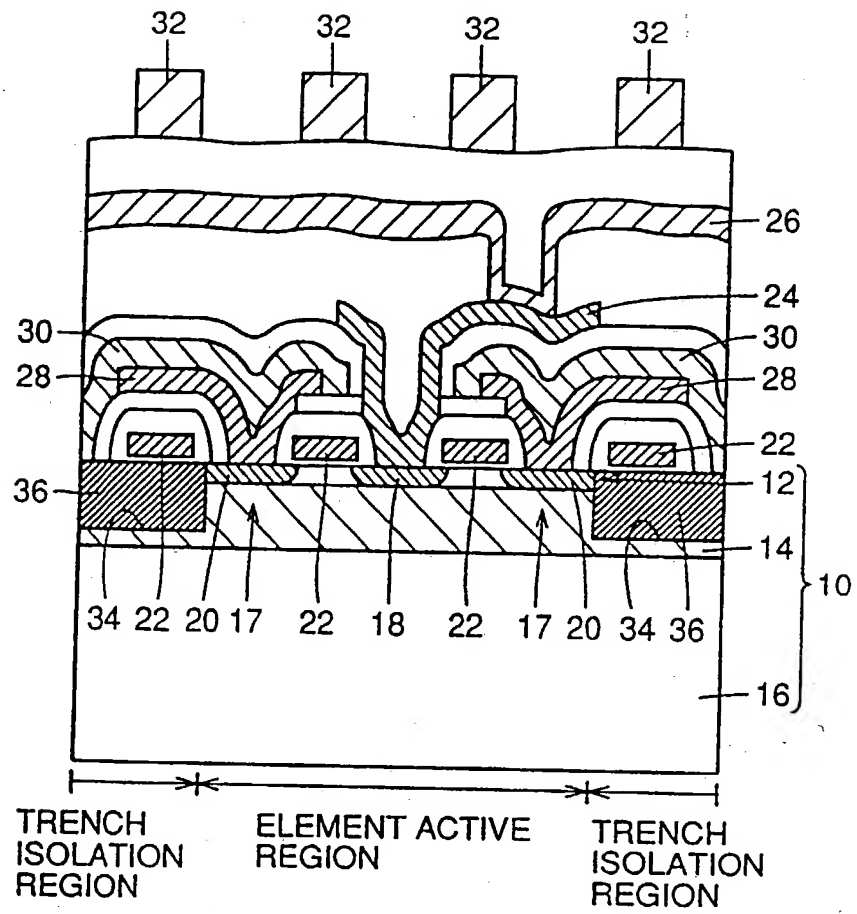


FIG. 3

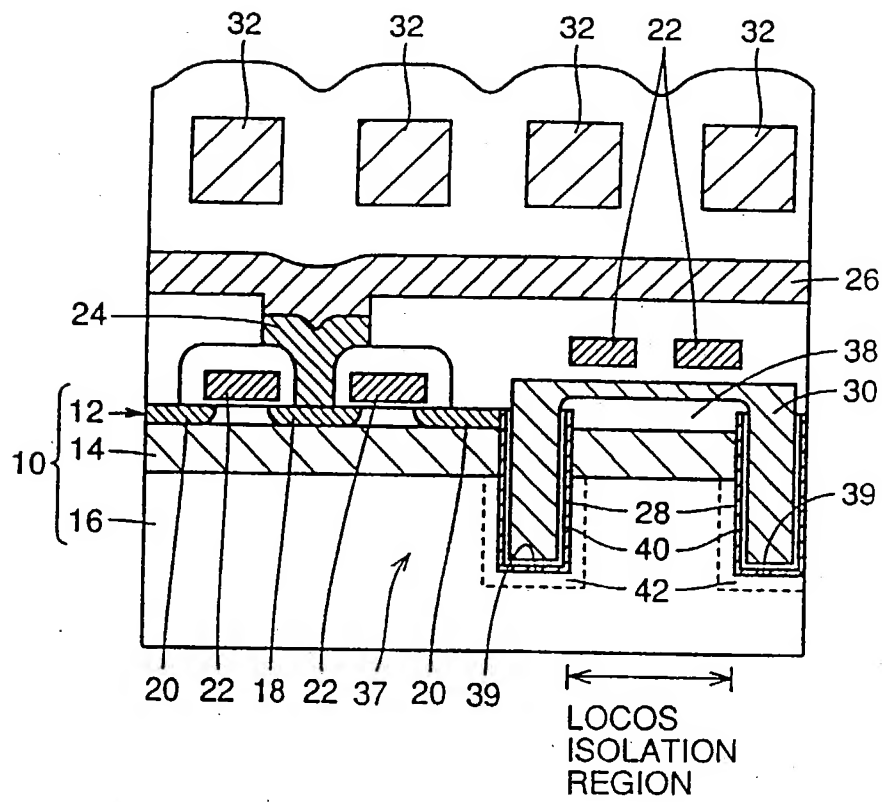
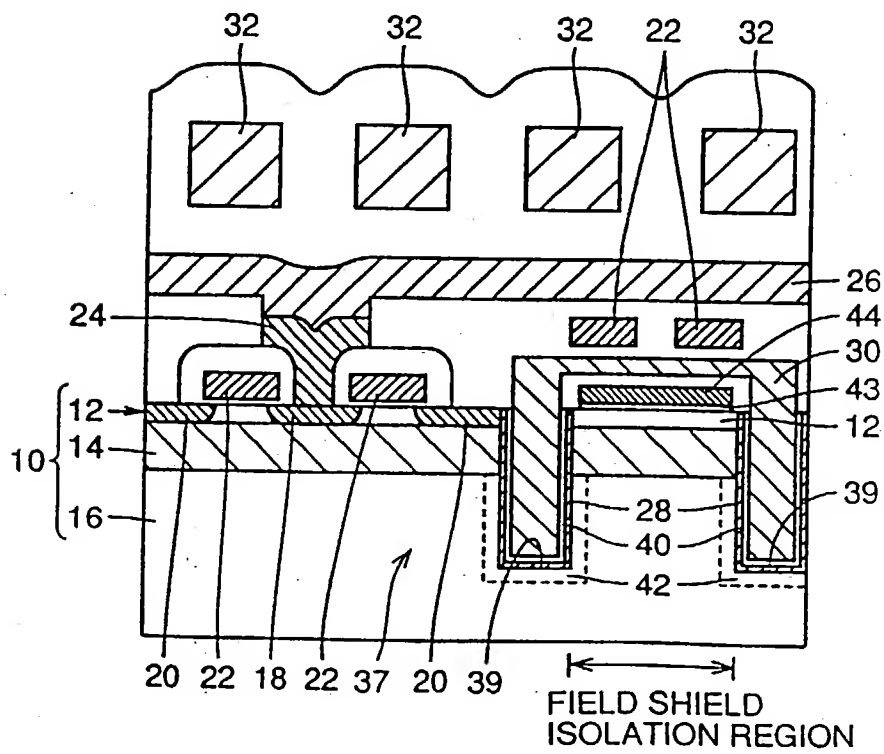


FIG. 4



This diagram is a cross-sectional view of a semiconductor device, labeled 10. It shows a substrate 16 with a series of layers: a base layer 12, a middle layer 14, and a top layer 26. A gate stack 24 is formed on the surface, with gate electrodes 22 and gate spacers 32. A field shield isolation region is defined by a dashed line 39, containing a rectangular structure 28 with a central core 40 and a surrounding layer 42. The region is labeled "FIELD SHIELD ISOLATION REGION" with a double-headed arrow. Other labels include 20, 18, 37, and 39, which point to various structural features and regions within the device.

[illegible]

**FIG. 8**

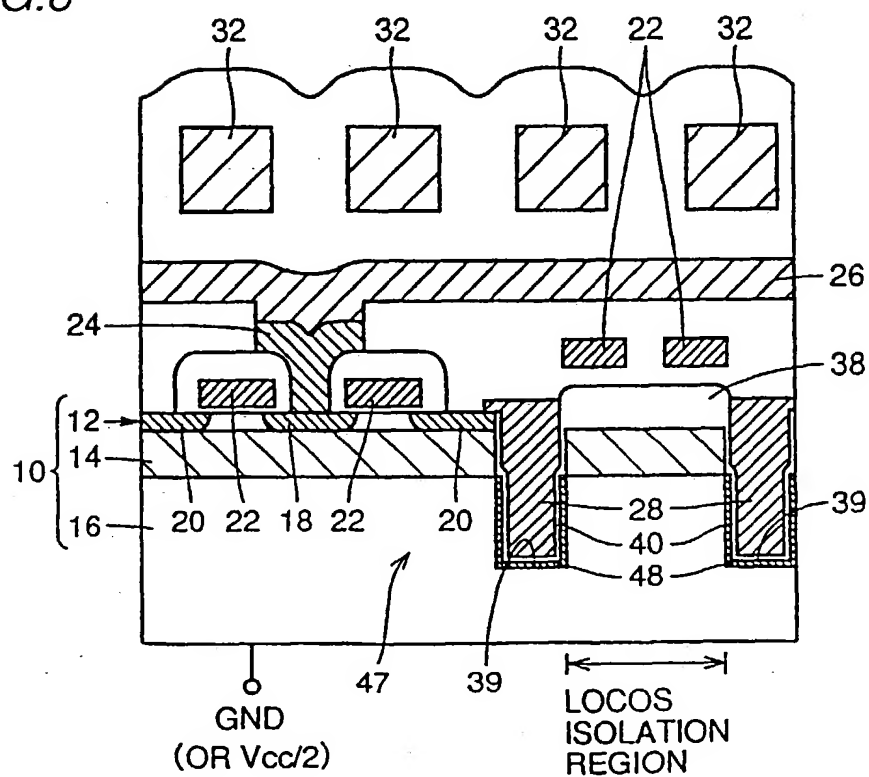


FIG.9

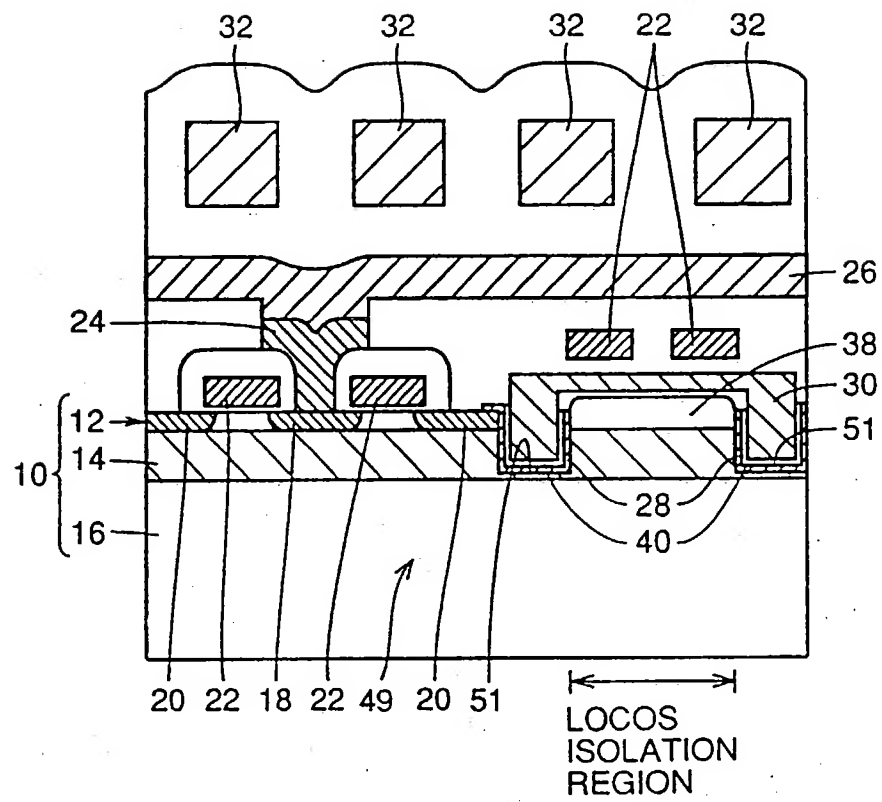


FIG.10

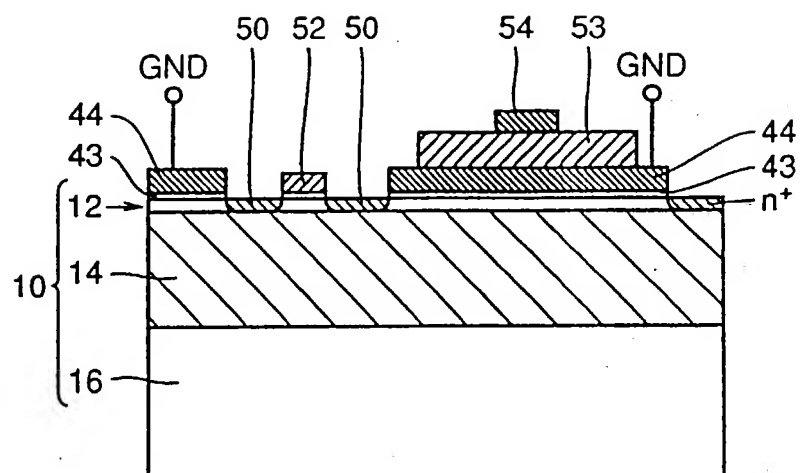


FIG.11

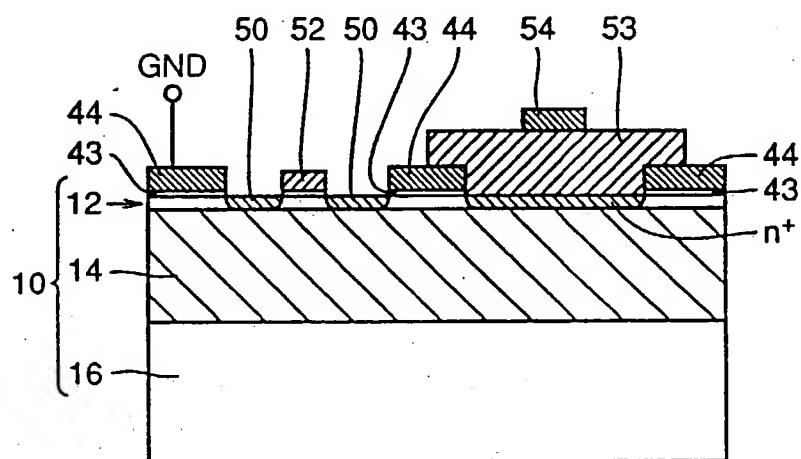


FIG.12

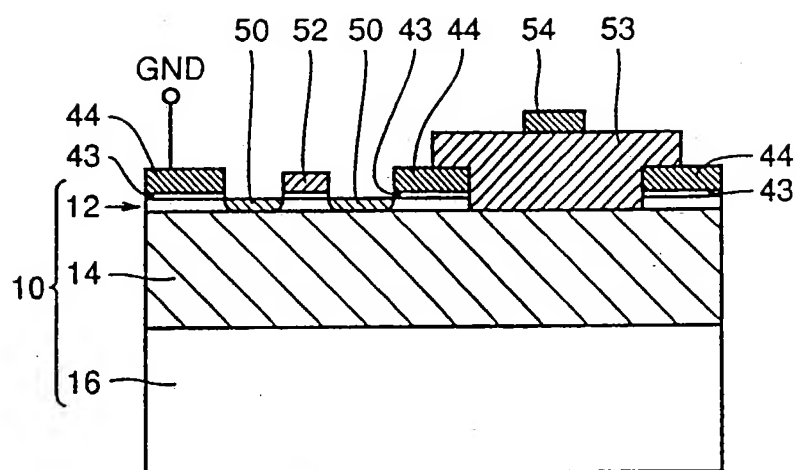


FIG.13

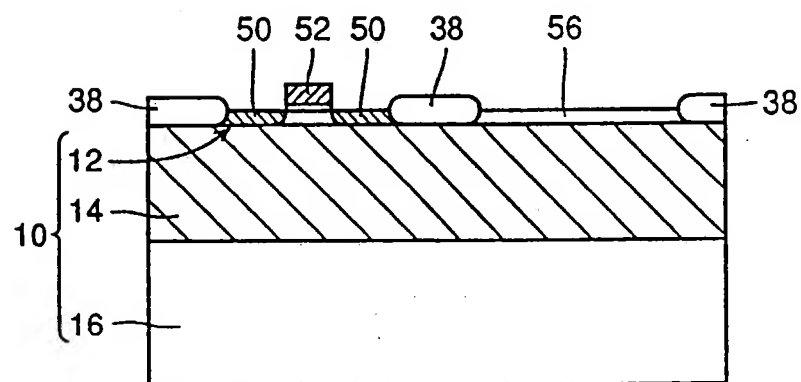




FIG. 14

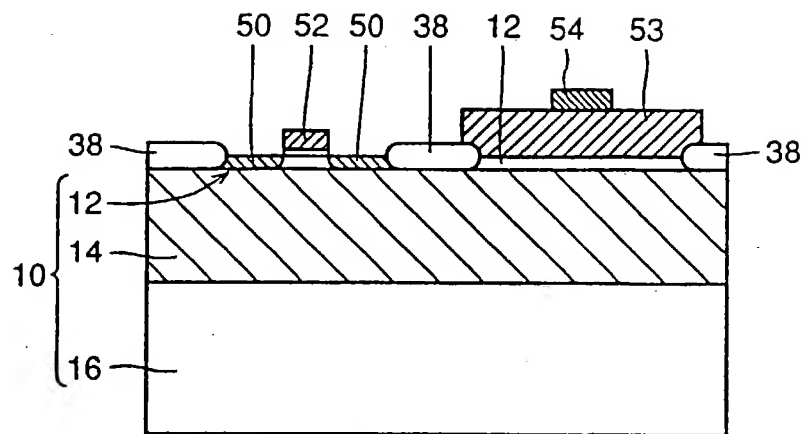


FIG. 15

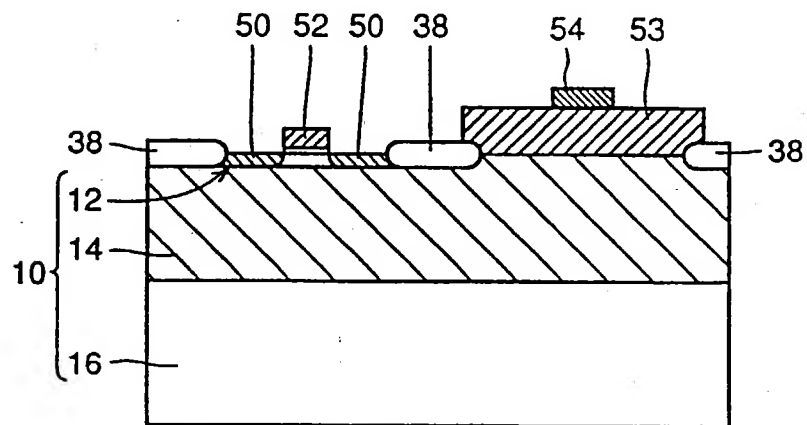


FIG. 16

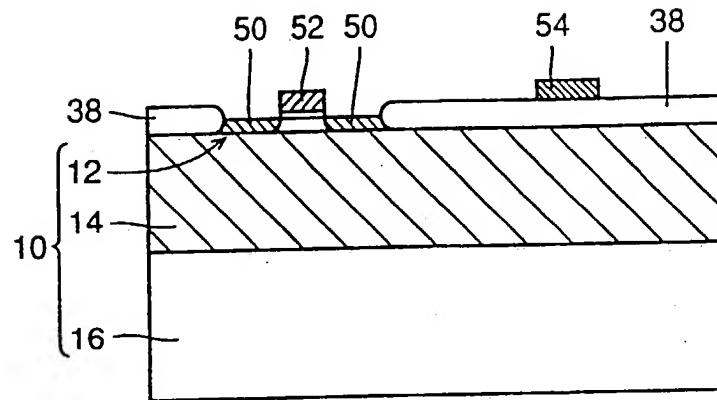


FIG. 17

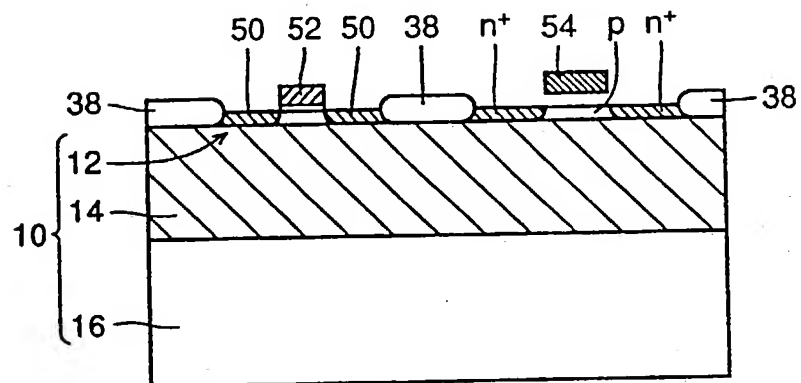


FIG. 18

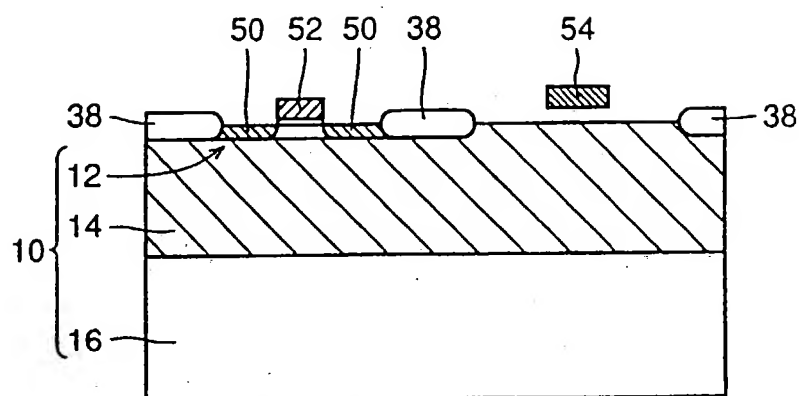


FIG.19

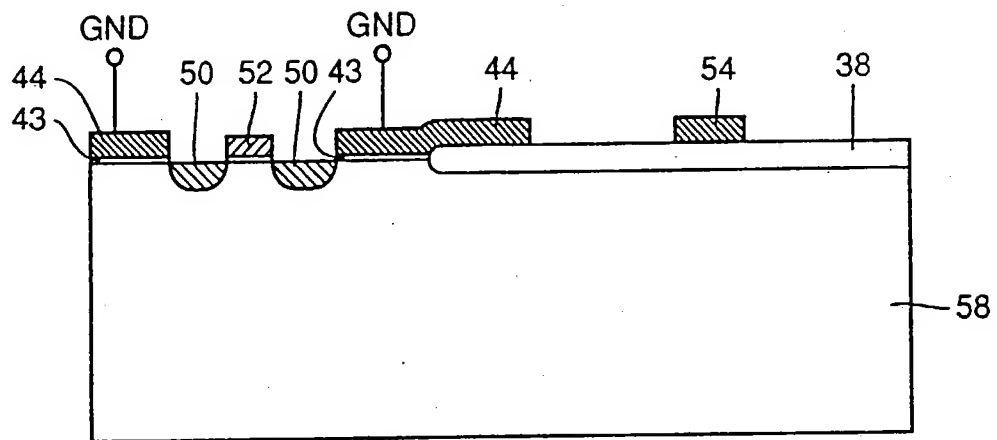


FIG.20

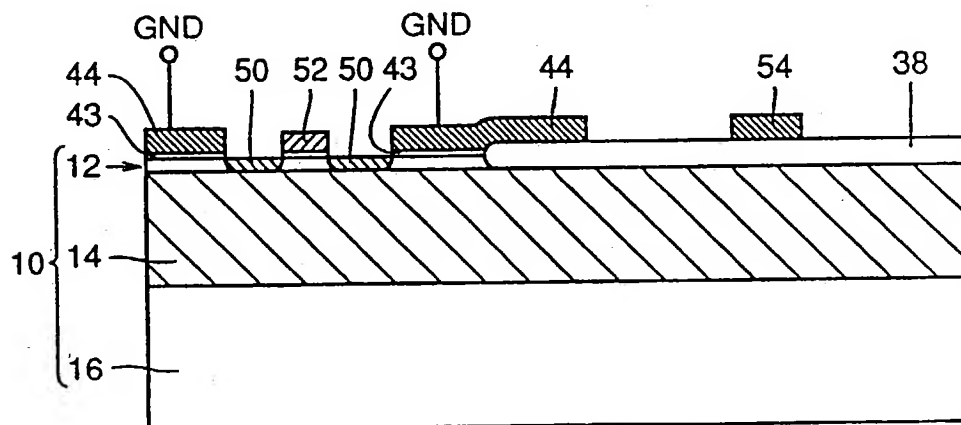


FIG.21

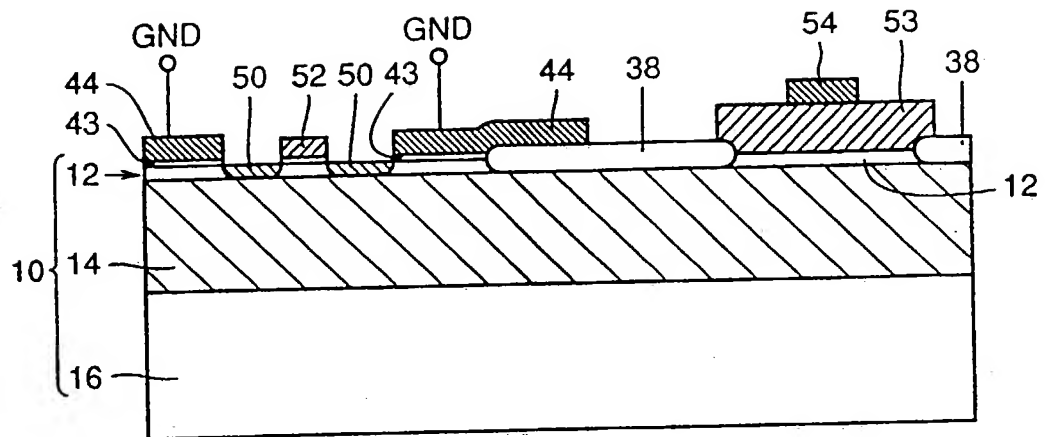


FIG.22

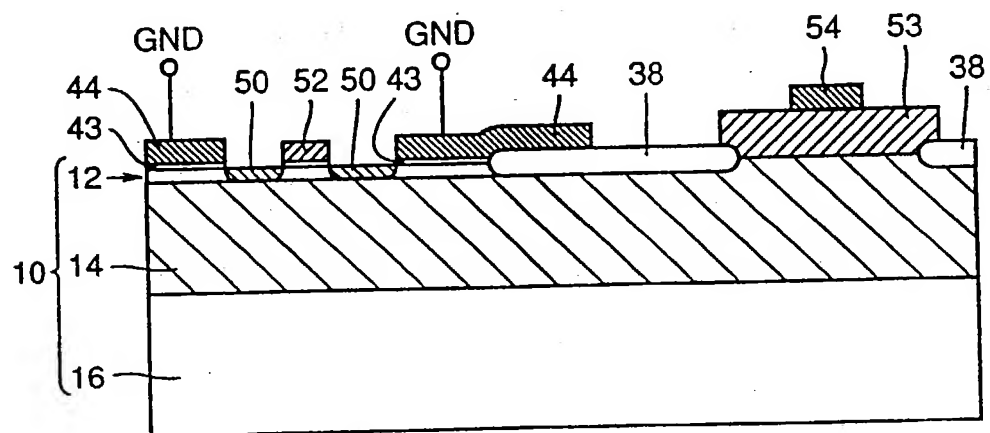


FIG.23

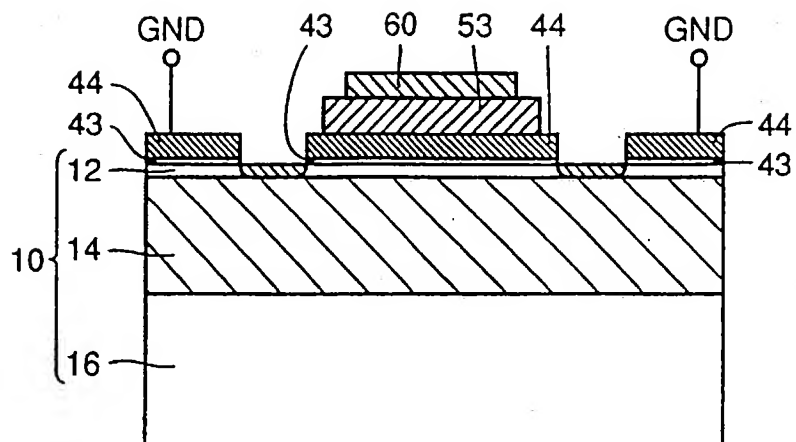


FIG.24

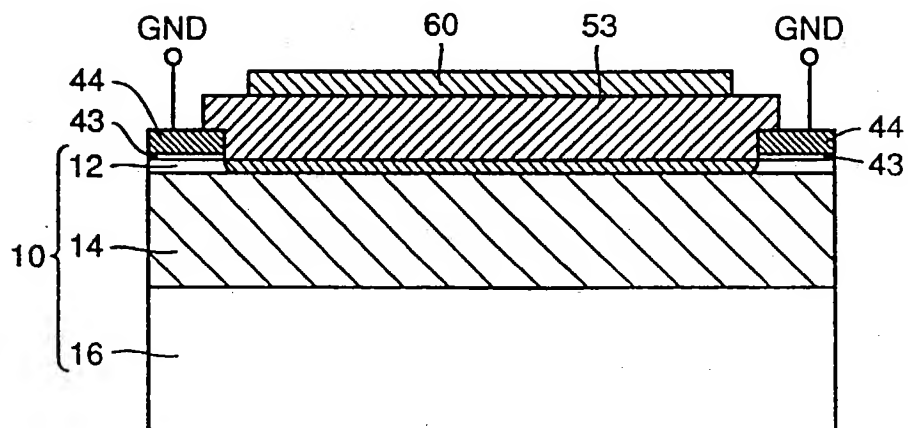


FIG.25

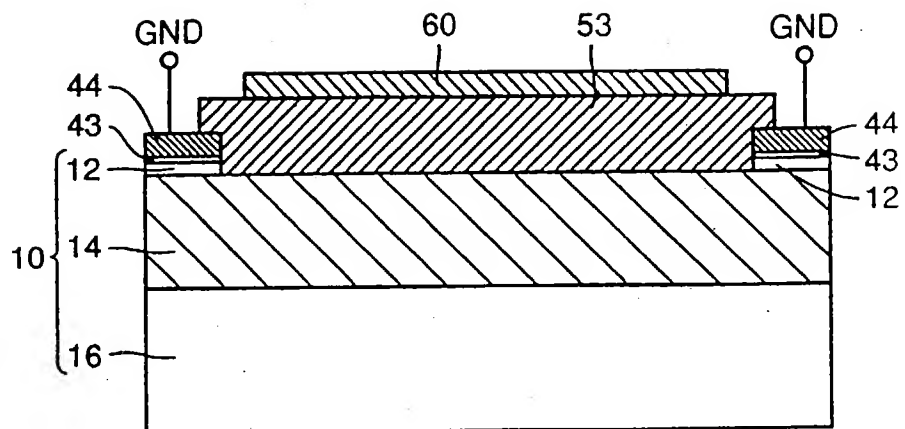


FIG.26

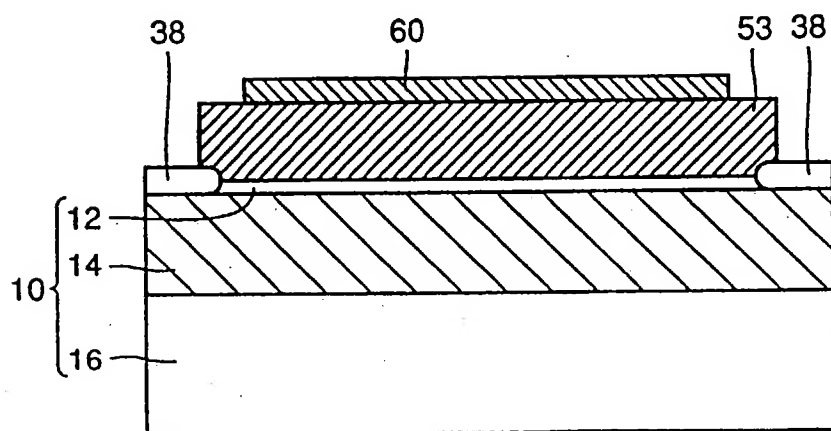


FIG.27

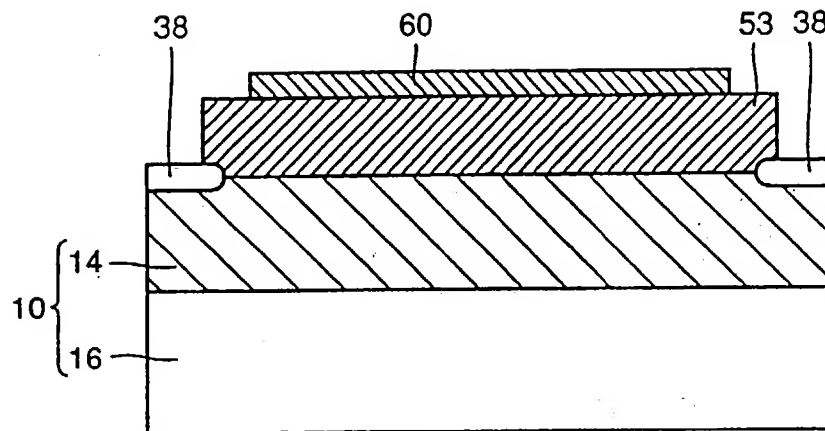




FIG.28

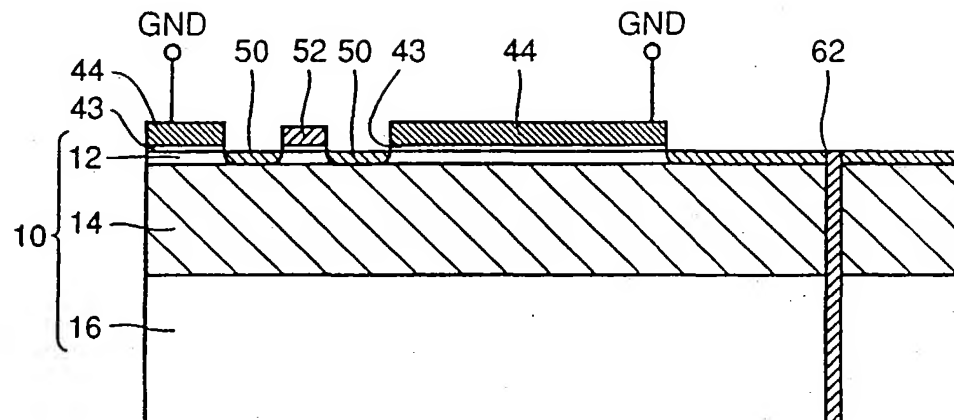


FIG.29

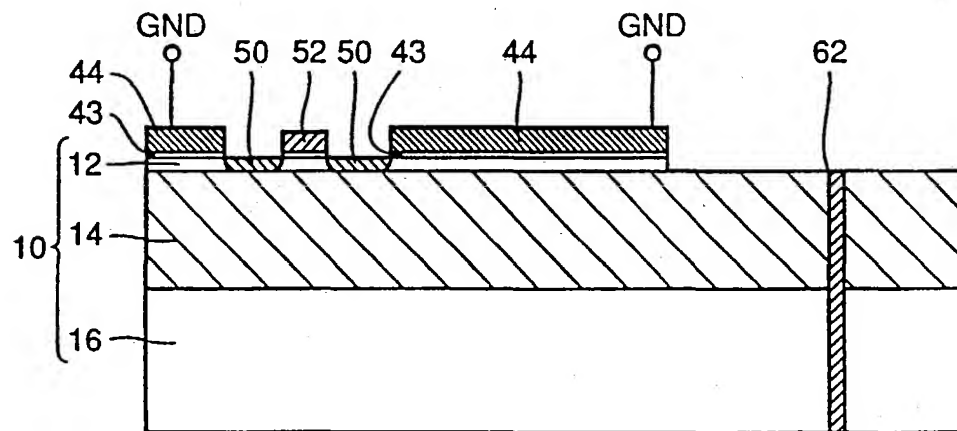


FIG.30

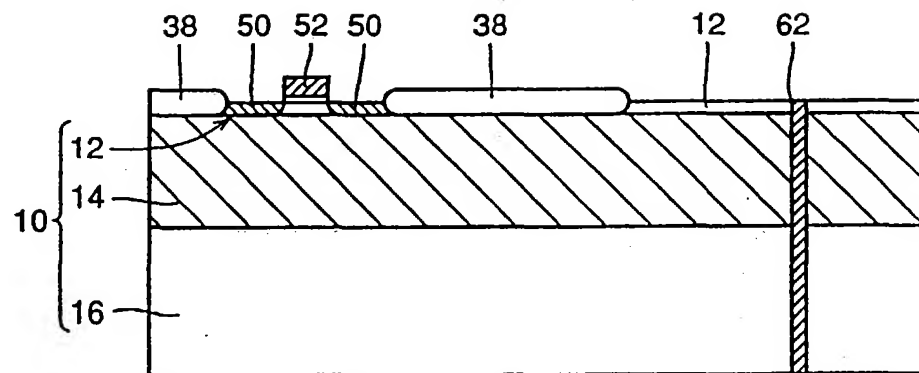


FIG.31

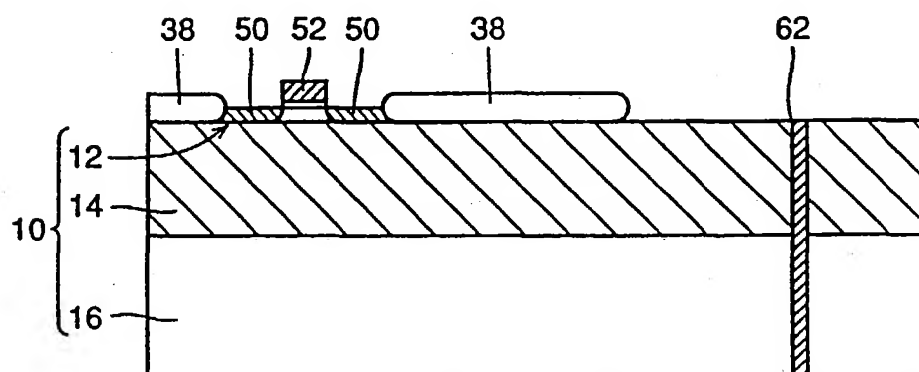


FIG.32

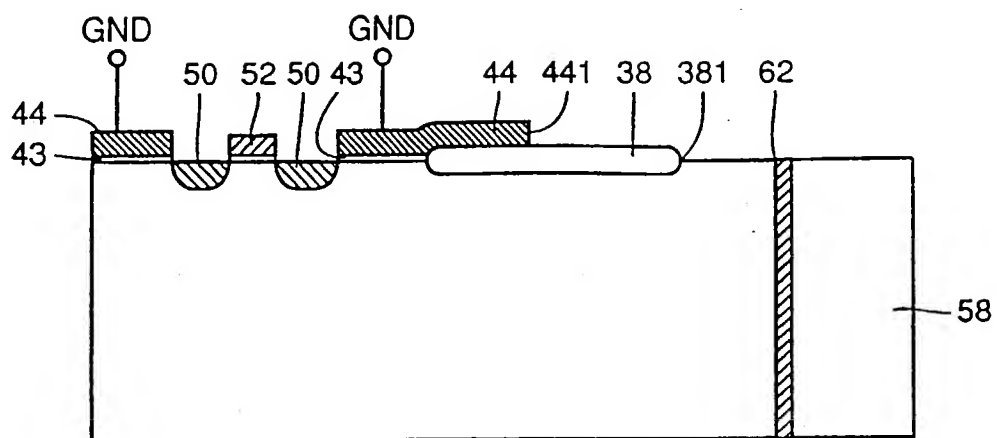


FIG.33

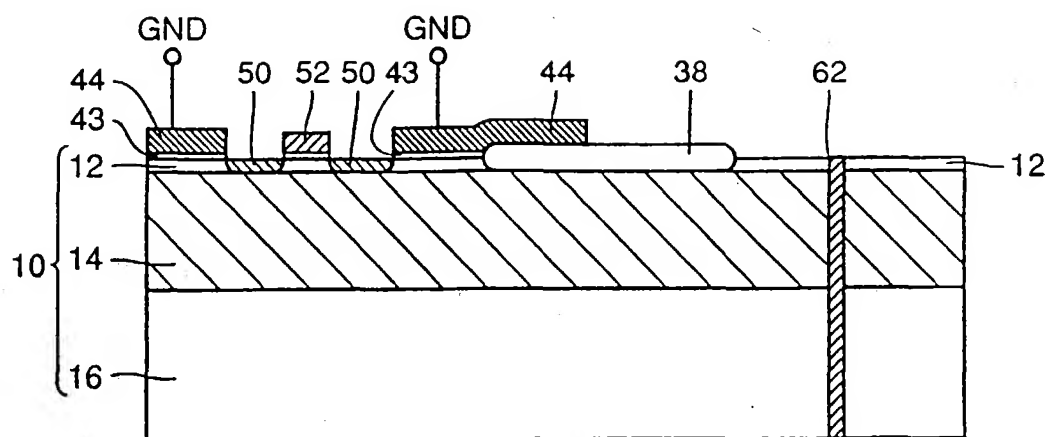


FIG.34

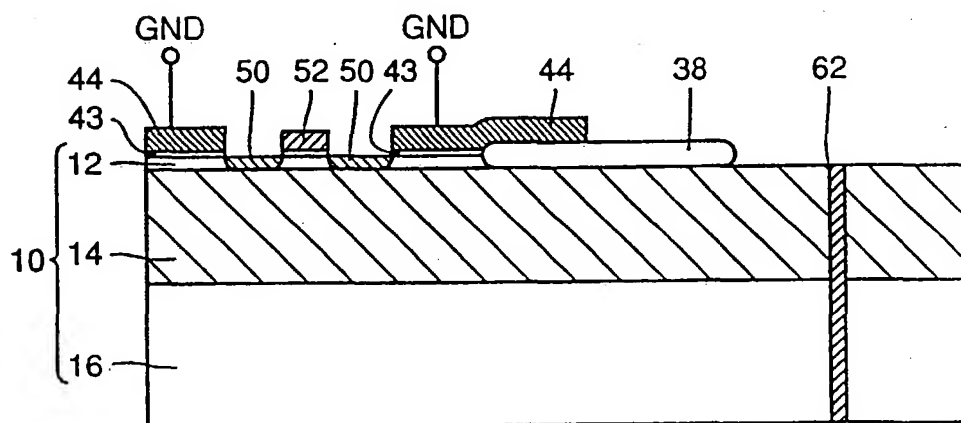


FIG.35

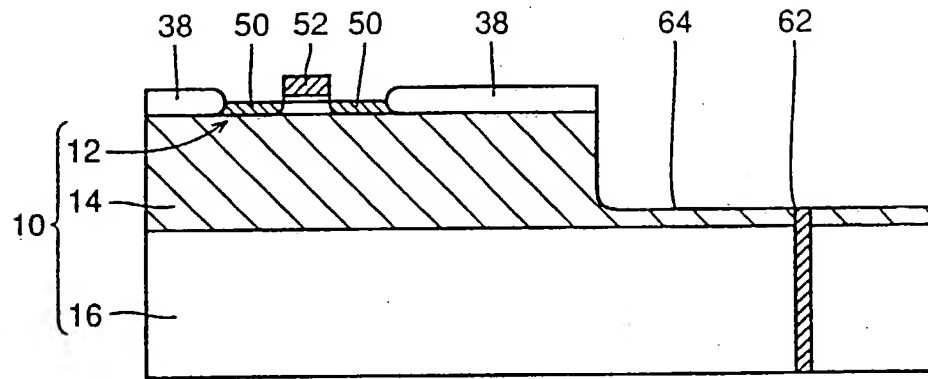


FIG.36

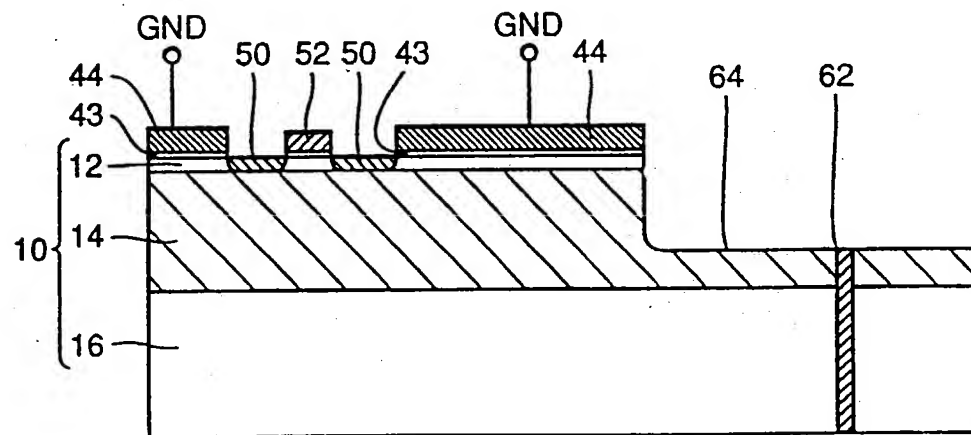
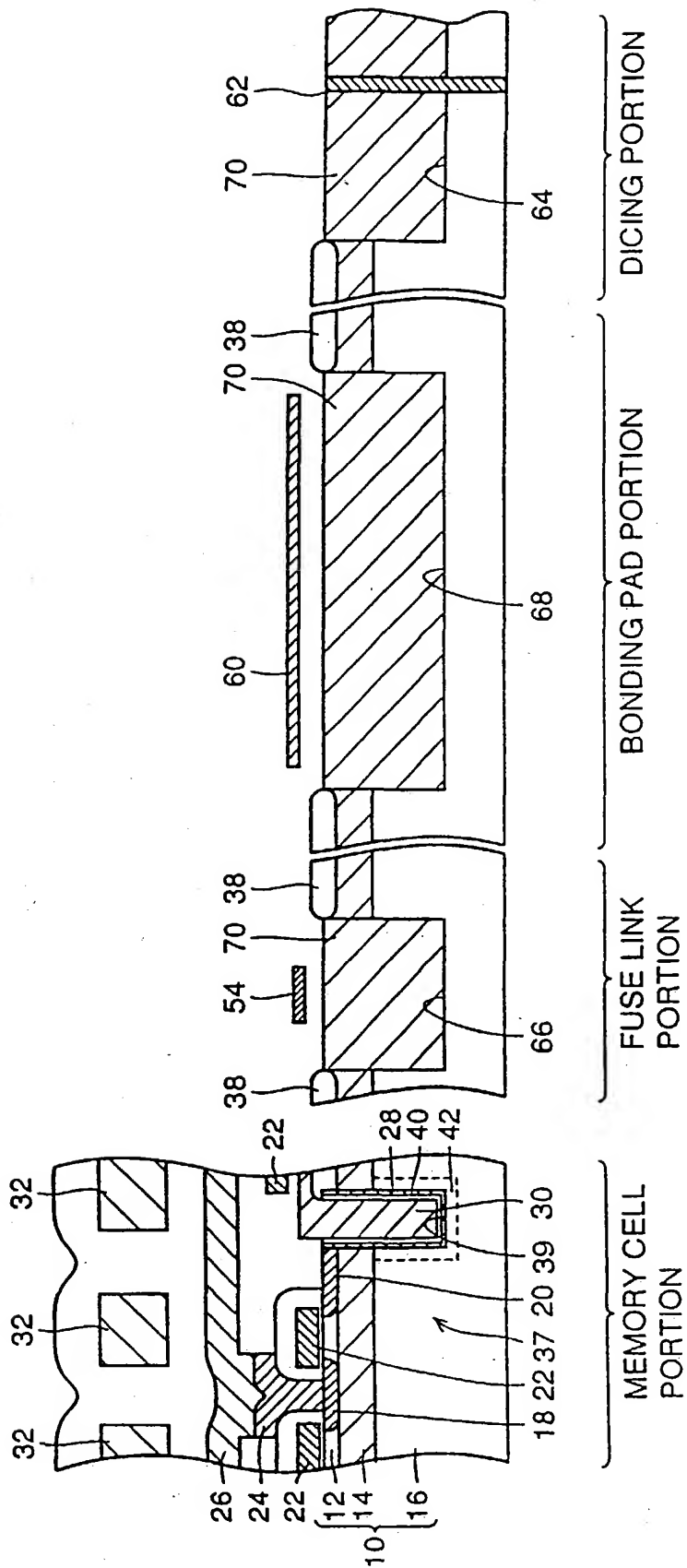


FIG.37



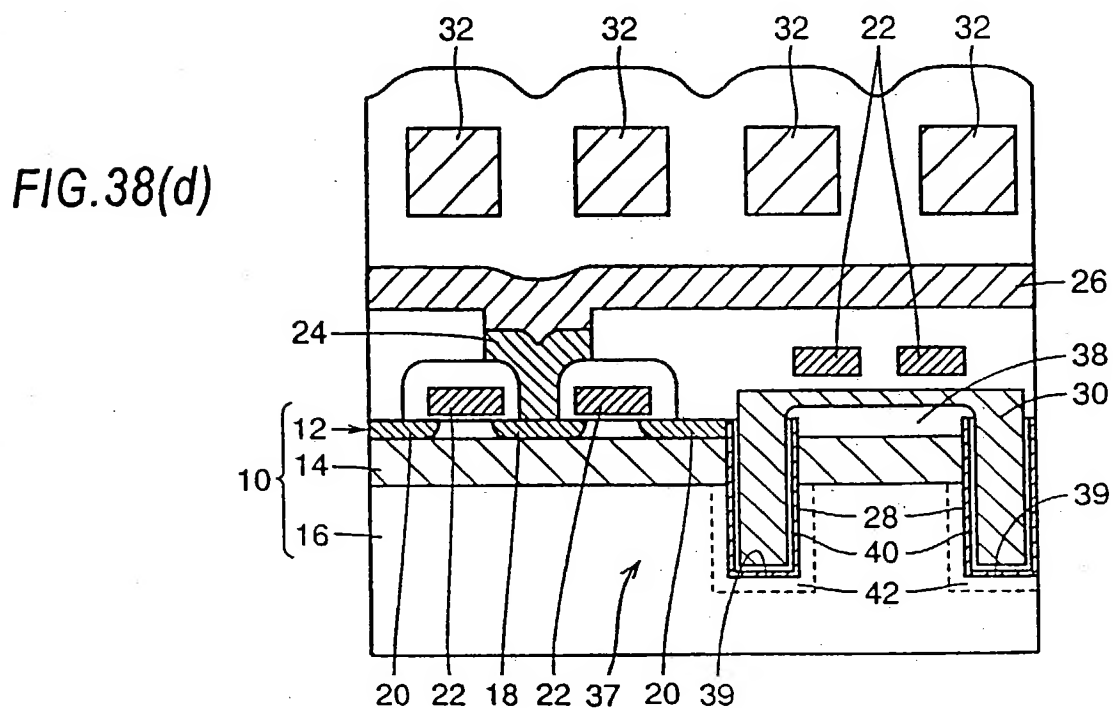
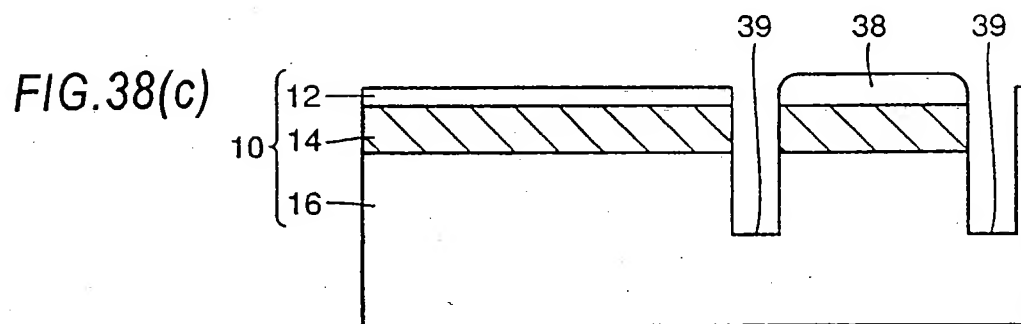
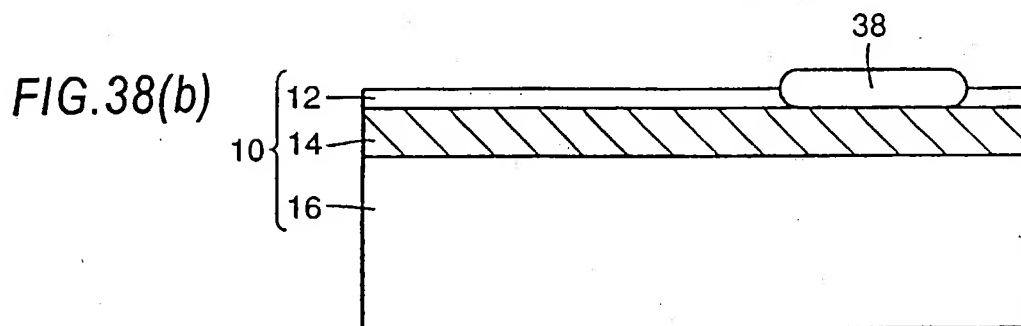
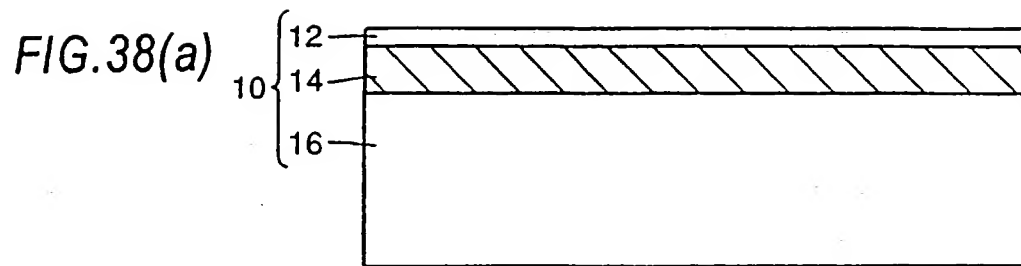


FIG.39(a)

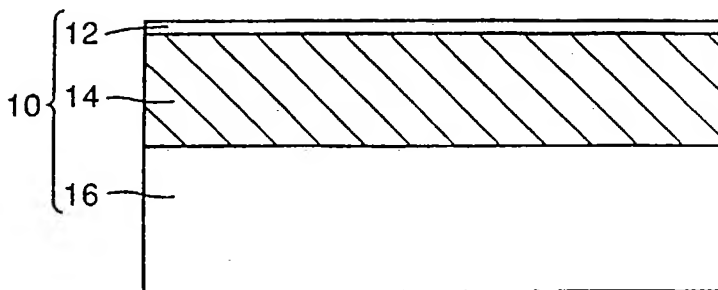


FIG.39(b)

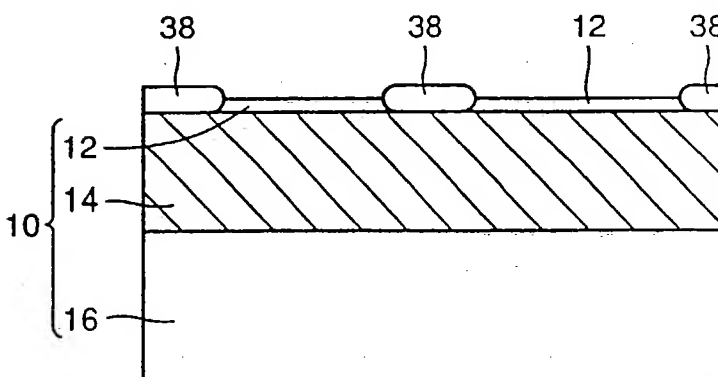


FIG.39(c)

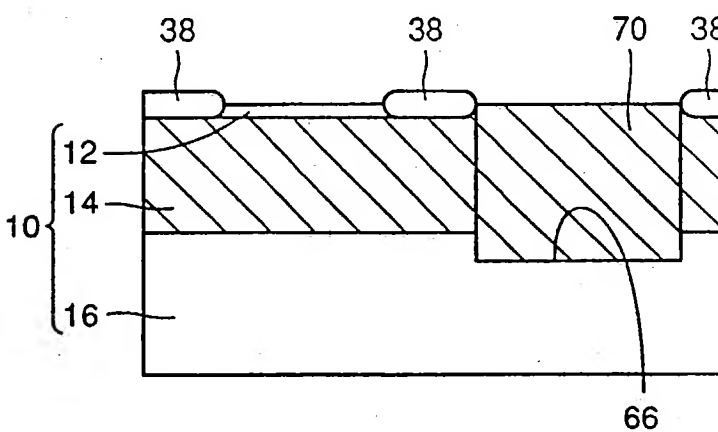


FIG.39(d)

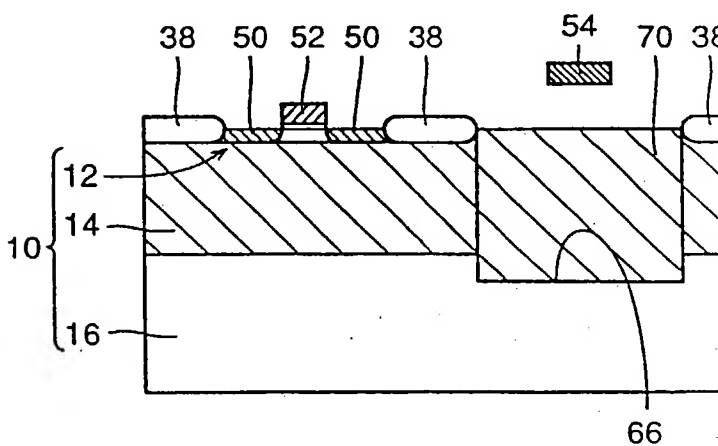




FIG. 40(a)

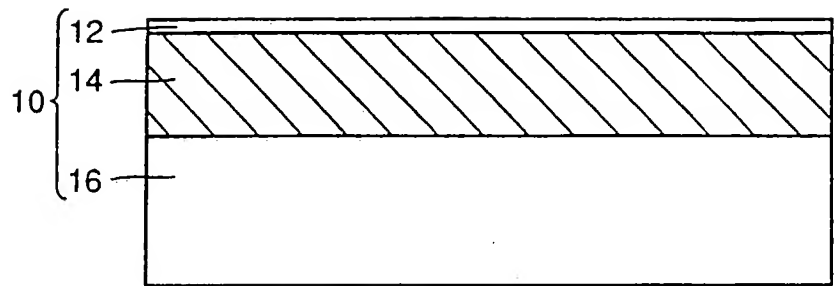


FIG. 40(b)

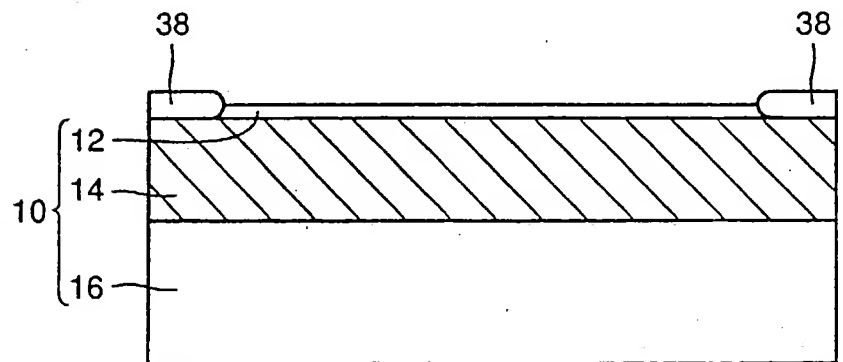


FIG. 40(c)

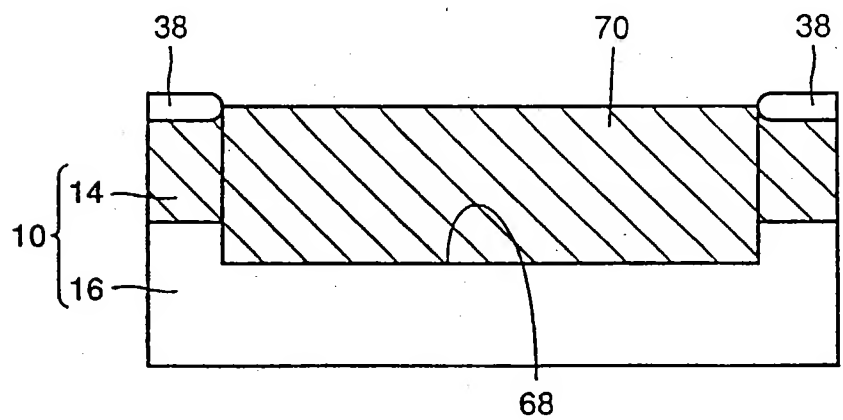


FIG. 40(d)

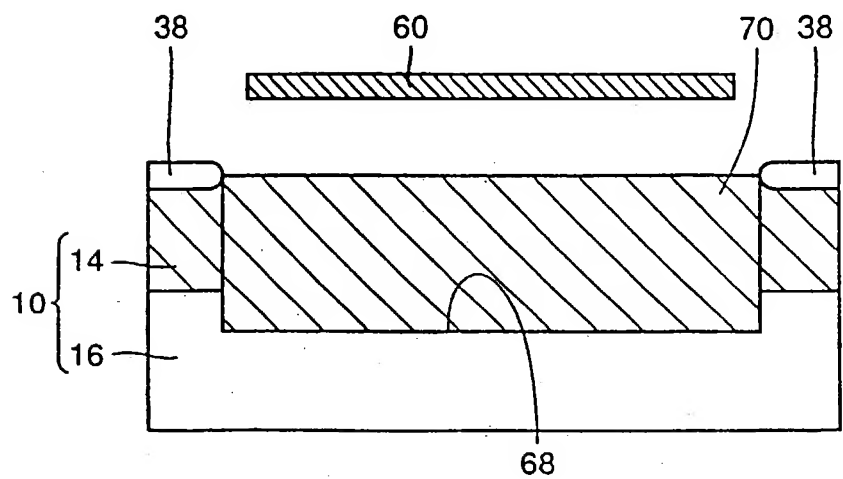


FIG.41(a)

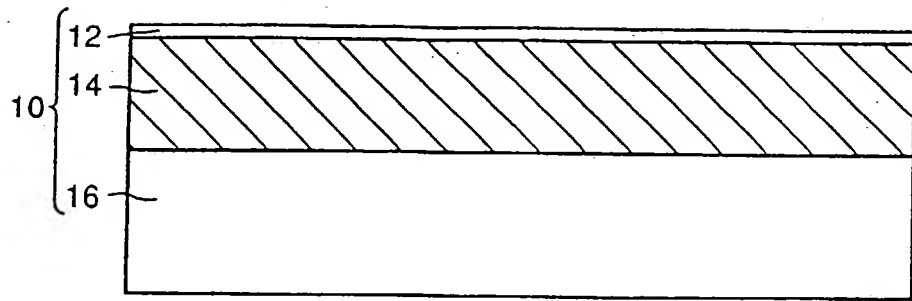


FIG.41(b)

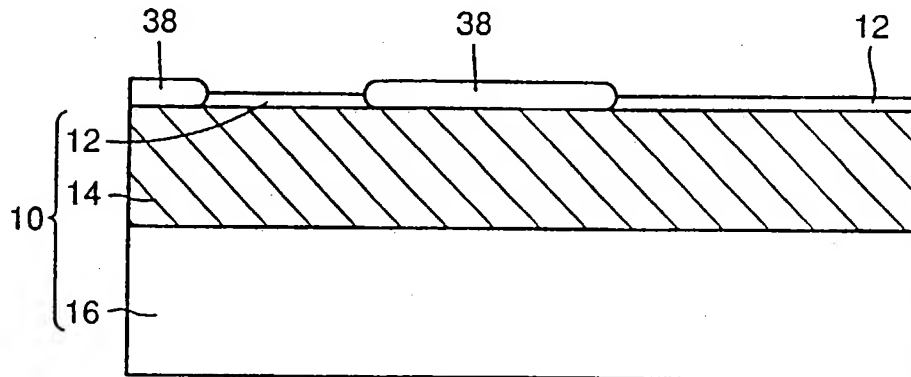


FIG.41(c)

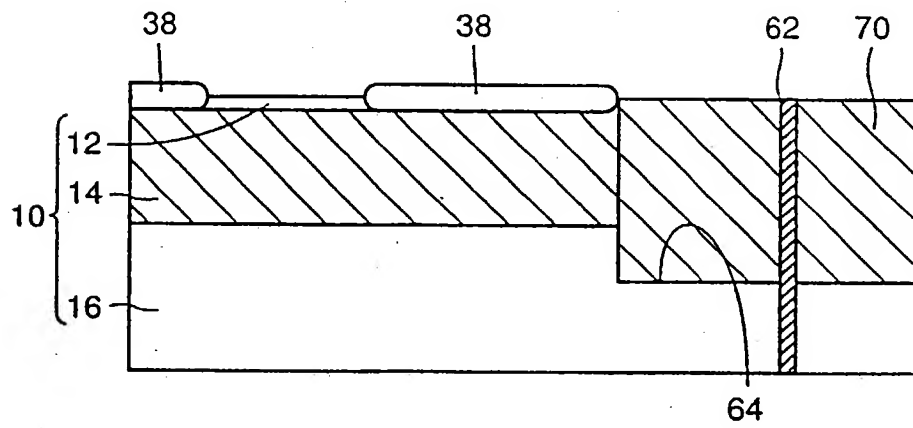


FIG.41(d)

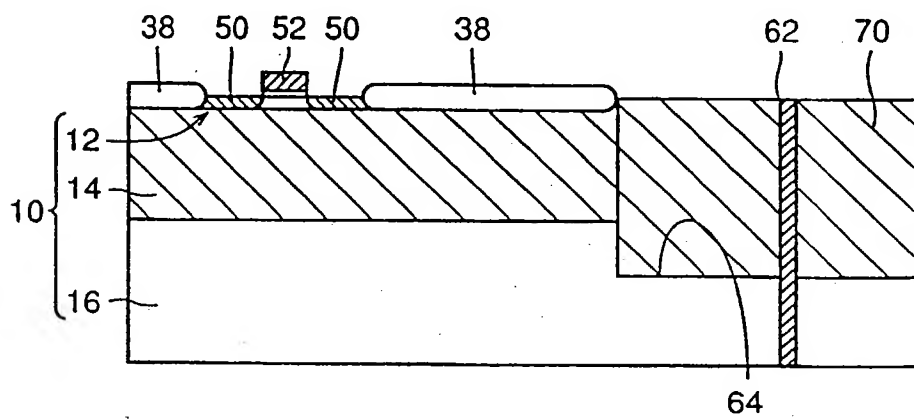


FIG. 42

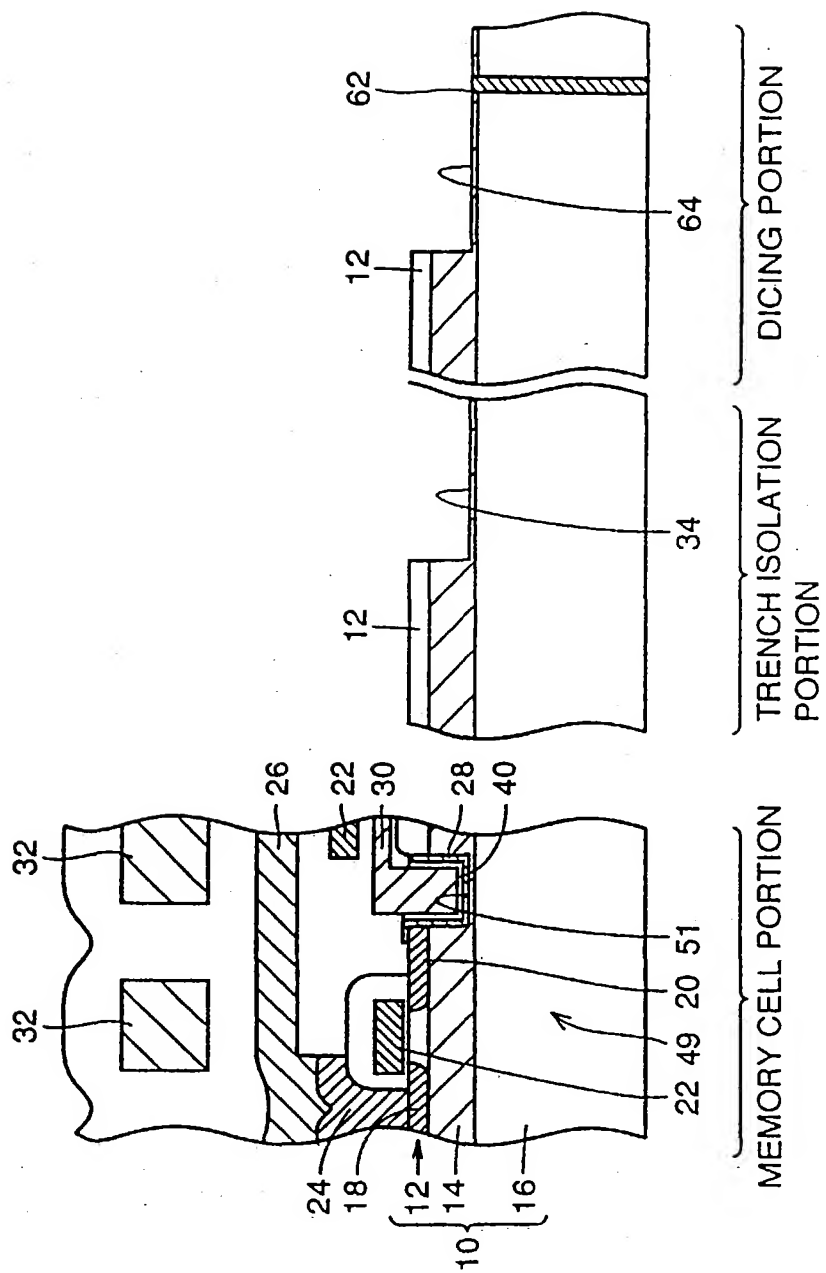


FIG. 43 PRIOR ART

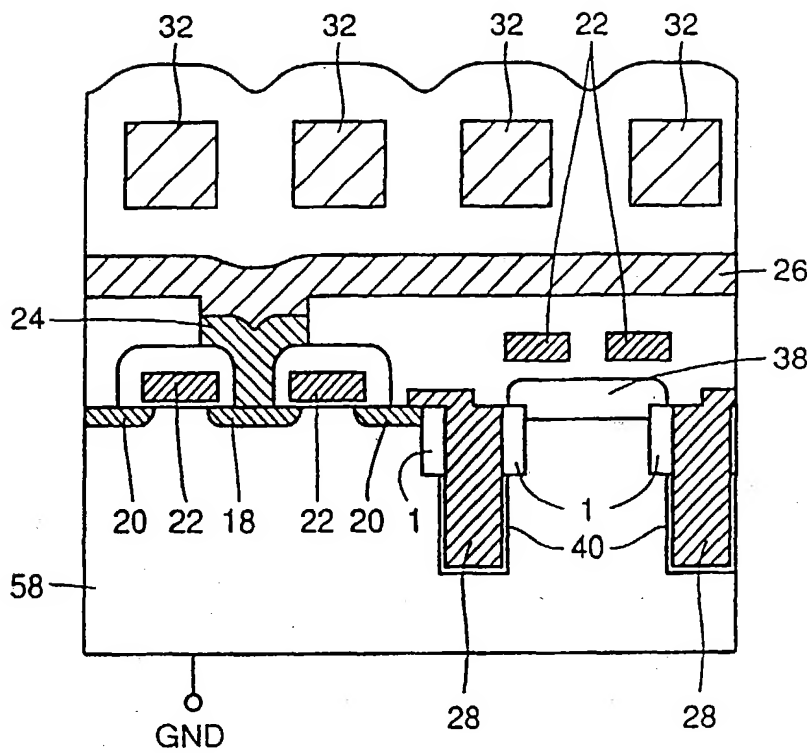


FIG.44 PRIOR ART

